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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/704,467	10/31/2000	Charles P. Roth	10559-286001	5582

20985 7590 06/16/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/16/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/704,467	Applicant(s) ROTH ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003 and 31 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16, 18-21, and 23 and new claims 24-30 have been considered. Claims 1-14, 16, 18-19, 21, and 23 have been amended as per Applicant's request. Claims 17 and 22 have been cancelled as per Applicant's request. New claims 24-30 have been added per Applicant's request.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9-14, 16-19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shang et al., U.S. Patent Number 5,941,980 (herein referred to as Shang) in view of Iizuka, U.S. Patent Number 5,299,321 (herein referred to as Iizuka) and in further view of Scantlin, U.S. Patent Number 5,574,927 (herein referred to as Scantlin).

4. Referring to claim 1, Shang has taught a method of providing instructions to a processor from an emulation instruction register comprising:

a. Determining a validity of a first instruction of the plurality of instructions by reading width bits in the first instruction (Shang Abstract; column 15, lines 20-61; and Figure 2);

b. Determining a validity of a second instruction of the plurality of instructions by reading width bits in the second instruction (Shang Abstract; column 15, lines 20-61; and Figure 2).

5. Shang has not explicitly taught:

a. Receiving a plurality of instructions simultaneously from the instruction register;

b. Providing the first instruction of the plurality of instructions to a decoder if the first instruction is valid;

c. Providing the second instruction of the plurality of instructions to the decoder if the second instruction is valid.

6. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Receiving a plurality of instructions simultaneously from the instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Providing the first instruction of the plurality of instructions to a decoder (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) if the first instruction is valid (Shang Abstract; column 15, lines 20-61; and Figure 2);

c. Providing the second instruction of the plurality of instructions to the decoder (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) if the second instruction is valid (Shang Abstract; column 15, lines 20-61; and Figure 2).

7. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to

increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

8. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

9. Referring to claim 2, Shang has taught determining the size of the plurality of instructions (Shang Abstract; column 15, lines 20-61; and Figure 2). In regards to Shang, the instruction size is needed in order to determine where the next instruction begins (Shang column 4, line 63 to column 5, line 7). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

10. Referring to claim 3, Shang has not explicitly taught storing the plurality of instructions in a single instruction register in subsequent clock cycles. However, Shang has taught use in a

superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) including storing the plurality of instructions in a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4). In regards to Shang and Iizuka, a superscalar processor is a pipelined processor, which means that it continually fetches and stores instructions to be executed. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

11. Referring to claim 4, Shang has taught receiving the second instruction of the plurality of instructions after determining the first instruction is invalid (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized

emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

12. Referring to claims 5 and 6, Shang has not explicitly taught:

a. Loading the plurality of instructions in parallel into the emulation instruction register (Applicant's claim 5) and

b. Providing the second instruction to the decoder after the first instruction is completed (Applicant's claim 6).

13. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) including:

a. Loading the plurality of instructions in parallel into the emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) and

b. Providing the second instruction to the decoder after the first instruction is completed (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

14. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of

ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

15. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

16. Referring to claim 7, Shang has taught providing the plurality of instructions to the decoder after a first run-test idle state without entering into a second run-test idle state (Shang Abstract; column 15, lines 20-61; and Figure 1). In regards to Shang, the idle state is entered and completed without a second idle state being entered since the corrected instructions are sent out when incorrect ones are identified. Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

17. Referring to claims 9 and 10, Shang has taught a method of processing instructions within a processor comprising receiving an RTI (Shang Abstract; column 1, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. Loading a plurality of instructions into a single instruction register (Applicant's claim 9);

b. Simultaneously providing the plurality of instructions to the processor (Applicant's claim 9); and

c. Processing the plurality of instructions (Applicant's claim 9).

d. Loading the plurality of instruction into an N-bit emulation instruction register (Applicant's claim 10).

18. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Loading a plurality of instructions into a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Simultaneously providing the plurality of instructions to the processor (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4); and

c. Processing the plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

d. Loading the plurality of instruction into an N-bit emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

19. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

20. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

21. Referring to claim 11, Shang has taught determining a validity of each of the plurality of instructions before processing (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

22. Referring to claim 12, Shang has taught aborting the processing of any invalid instructions and loading a next instruction of the plurality of instructions from the instruction register (Shang Abstract; column 15, lines 20-61; and Figure 2).

23. Referring to claim 13, Shang has taught loading a next instruction of the plurality of instructions from the instruction register if a no-operation instruction is loaded (Shang Abstract; column 15, lines 20-61; and Figure 2).

24. Referring to claim 14, Shang has taught providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Shang Abstract; column 15, lines 20-61; and Figure 2).

25. Referring to claim 16, Shang has taught a processor comprising emulation control logic adapted to control a flow of the plurality of instructions to a processor pipeline following detection of a single run-test idle state (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. An instruction register adapted to store a plurality of instructions,

b. A decoder to receive the plurality of instructions for processing.

26. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. An instruction register adapted to store a plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4),

b. A decoder which may receive the plurality of instructions for processing (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

27. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

28. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

29. Referring to claim 18, Shang has taught wherein the control logic determines a validity of the plurality of instructions by reading bits in each instruction indicating a width of each instruction and discards any invalid instructions (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1,

lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

30. Referring to claim 19, Shang has taught wherein the control logic loads a next instruction from the instruction register immediately after detecting a no-operation instruction (Shang Abstract; column 16, lines 20-61; and Figure 2). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

31. Referring to claim 21, Shang has taught an apparatus, including instructions residing on a machine-readable storage medium, for use in a device to handle a plurality of instructions, the operating instructions pausing the device to enter a run-test idle state (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. Load the plurality of instructions into a single instruction register;

b. Provide the plurality of instructions to a processor; and

c. Process the plurality of instructions.

32. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Load the plurality of instructions into a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Provide the plurality of instructions to a processor (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4); and

c. Process the plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

33. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

34. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary

skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

35. Referring to claim 23, Shang has taught wherein the validity of each of the plurality of instructions is determined before processing by reading bits in each instruction indicating a width of each instruction (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

36. Referring to claims 24, 26, and 28-30, Shang has not taught has not taught

a. Scanning emulation instruction from an in-circuit emulator (ICE) to a Joint Test Action Group (JTAG) interface (Applicant's claim 24); and

b. Loading emulation instruction from the JTAG interface to the emulation instruction register (Applicant's claim 24).

c. Wherein the instruction register comprises first and second register (Applicant's claim 26).

d. A multiplexer to select between an emulation instruction for the plurality of emulation instruction to send to the processor pipeline (Applicant's claim 28).

e. An in-circuit emulator to monitor operations of the processor (Applicant's claim 29).

f. Executing at least one of the plurality of emulation instructions to monitor operation of the processor (Applicant's claim 30).

37. Scantlin has taught

a. Scanning emulation instruction from an in-circuit emulator (ICE) to a Joint Test Action Group (JTAG) interface (Scantlin column 4, line 34 to column 5, line 27 and Figure 2); and

b. Loading emulation instruction from the JTAG interface to the emulation instruction register (Scantlin column 4, line 34 to column 5, line 27 and Figure 2).

c. Wherein the instruction register comprises first and second register (Scantlin column 4, line 34 to column 5, line 27 and Figure 2).

d. A multiplexer to select between an emulation instruction for the plurality of emulation instruction to send to the processor pipeline (Scantlin column 4, line 34 to column 5, line 27 and Figure 2).

e. An in-circuit emulator to monitor operations of the processor (Scantlin column 4, line 34 to column 5, line 27 and Figure 2).

f. Executing at least one of the plurality of emulation instructions to monitor operation of the processor (Scantlin column 1, lines 49-53).

38. A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have

been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

39. Referring to claim 25, Shang has taught wherein a pre-determined set of width bits indicates an instruction is valid (Shang Abstract; column 15, lines 20-61; and Figure 2).

40. Claims 8, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shang in view of Iizuka and in further view of Scantlin, as applied to claims 1, 9, and 16 above, and further in view of Applicant's admitted prior art (herein referred to Prior Art).

41. Referring to claims 8 and 15, Shang in view of Iizuka has not explicitly taught providing first and second instructions to a digital signal processor. However, Shang has taught execution units with specific purposes (Shang column 1, lines 28-33). Prior Art has taught providing instructions to a digital signal processor (Prior Art page 1, line 19 to page 2, line 2). A person of ordinary skill at the time the invention was made would have recognized that DSPs are more efficient at processing multimedia applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the DSP of Prior Art in the device of Shang in view of Iizuka in order to more efficiently complete processing of multimedia applications.

42. In addition, Shang has not taught emulation. Scantlin has taught emulation (Scantlin column 1, lines 34-53 and column 2, line 58 to column 3, line 25). A person of ordinary skill in the art at the time the invention was made, and as taught by Scantlin, would have recognized emulation increases compatibility between processors and software as well as lowering costs (Scantlin column 1, lines 49-53). Therefore, it would have been obvious to a person of ordinary

skill in the art at the time the invention was made to incorporate the emulation of Scantlin in the device of Shang to increase compatibility and lower costs.

43. Referring to claim 20, Shang has not explicitly taught wherein the processor is a digital signal processor. However, Shang in view has taught execution units with specific purposes (Shang column 1, lines 28-33). Prior Art has taught wherein the processor is a digital signal processor (Prior Art page 1, line 19 to page 2, line 2). A person of ordinary skill at the time the invention was made would have recognized that DSPs are more efficient at processing multimedia applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the DSP of Prior Art in the device of Shang in view of Iizuka in order to more efficiently complete processing of multimedia applications.

44. Claims 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shang in view of Iizuka and in further view of Scantlin, as applied to claim 16 above, and further in view of Free On-line Dictionary of Computing ©1998 (herein referred to as FOLDOC). Shang has not explicitly taught wherein the emulation control logic comprises a state machine. However, Shang has taught that the device is somehow controls and determines the different states provided by the length determination device (Shang Abstract; column 15, lines 20-61; and Figure 2), FOLDOC has taught that state machines are a method of controlling a device with different states (FOLDOC state machine). A person of ordinary skill in the art at the time the invention was made would have recognized that a state machine is a convenient, effective, and highly common way to define and control different states to a device. Therefore, it would have been

obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the state machine of FOLDOC in the device of Shang.

Response to Arguments

45. Examiner withdraws the drawing objection in favor of amendment to the specification.

46. Examiner withdraws the specification objection in favor of amendments made to the title.

47. Examiner withdraws the 112 Rejection in favor of the claim amendments.

48. Applicant's arguments with respect to claims 1-16,18-21 and 23-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Dye et al., U.S. Patent Number 5,249,266, has taught emulation.

50. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

51. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

52. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

53. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

54. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
June 14, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100